

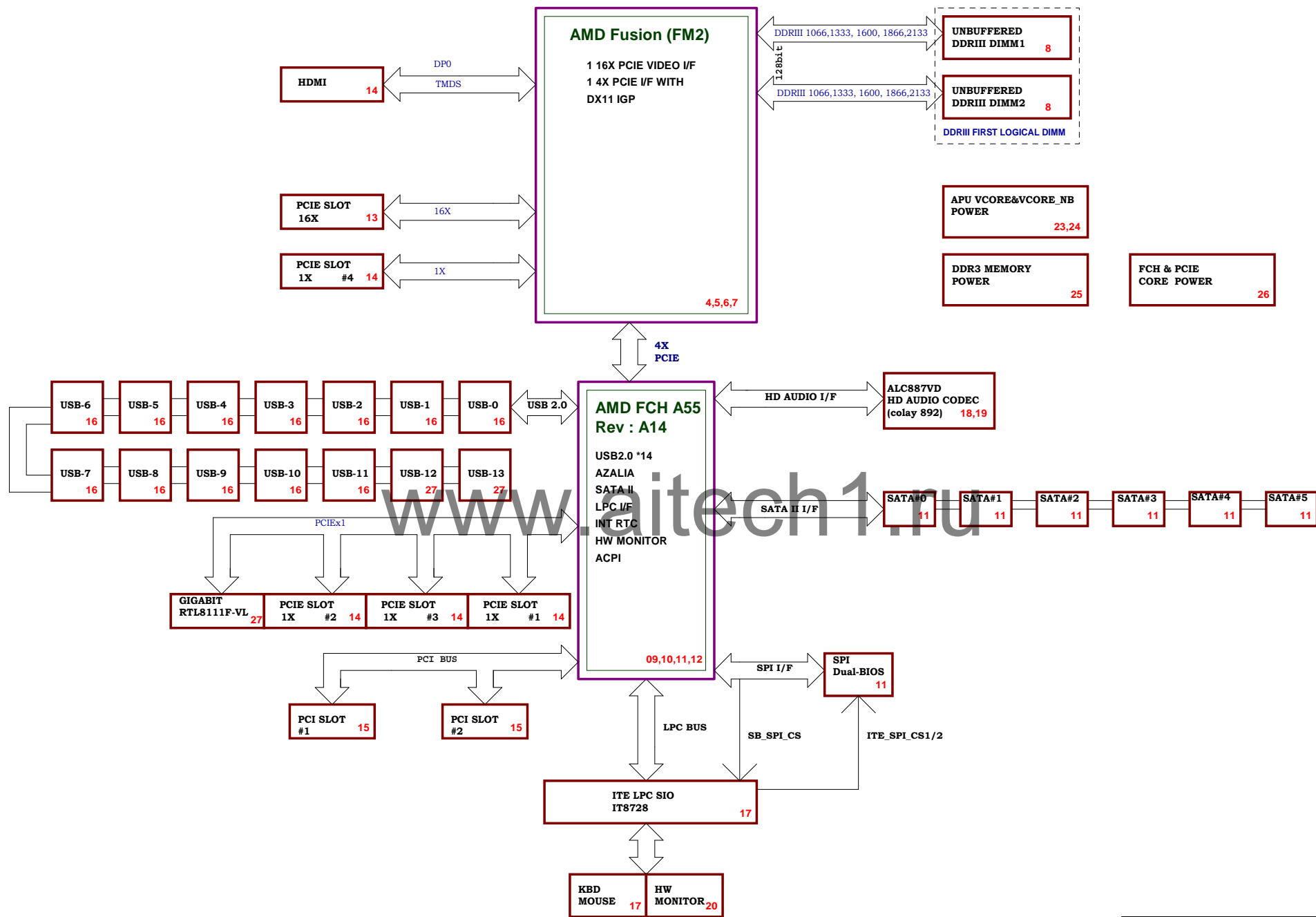
Component value change history

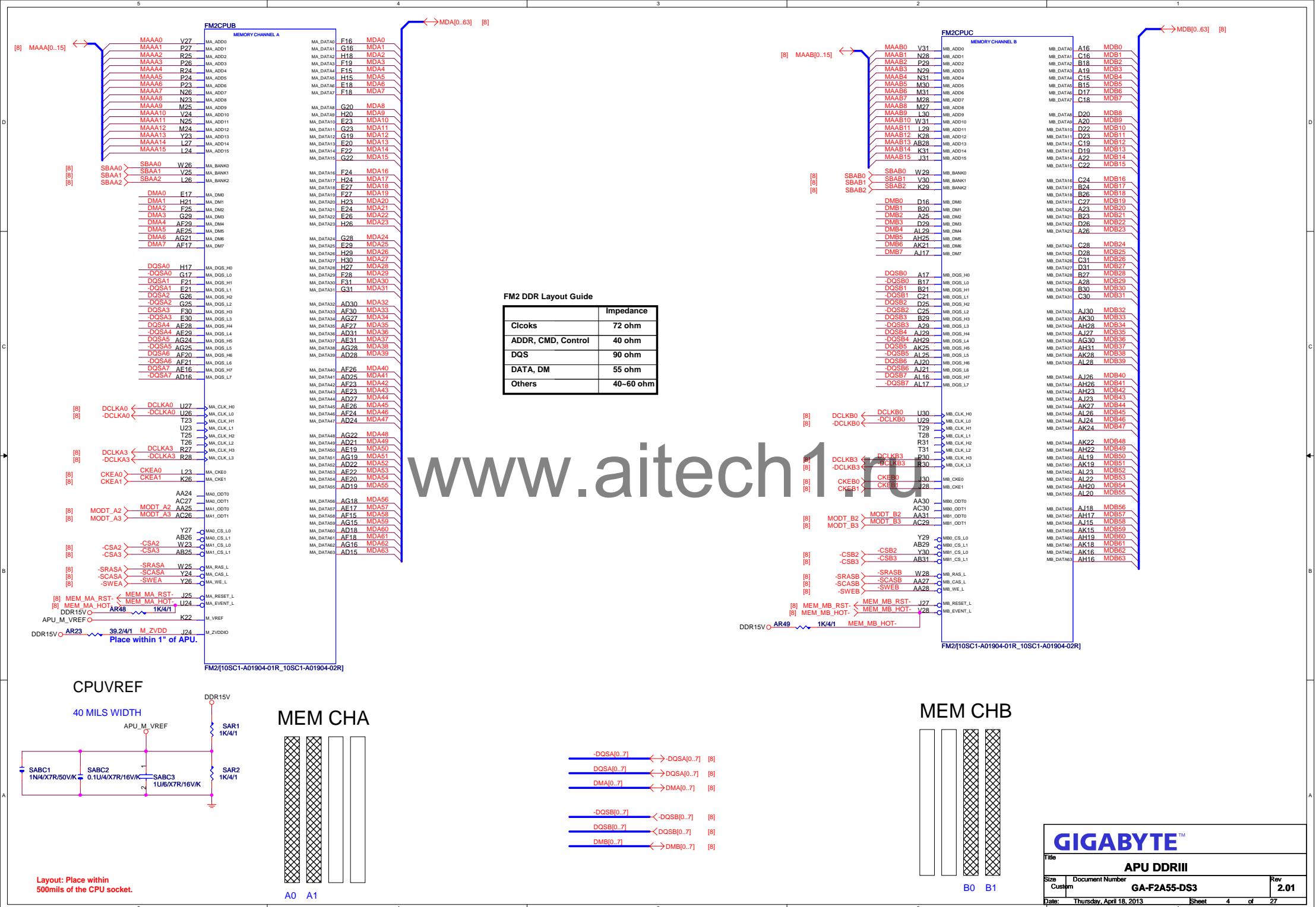
P-Code : U12031-0
Tip/Top : 9MF255DS3-00

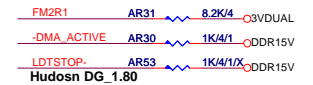
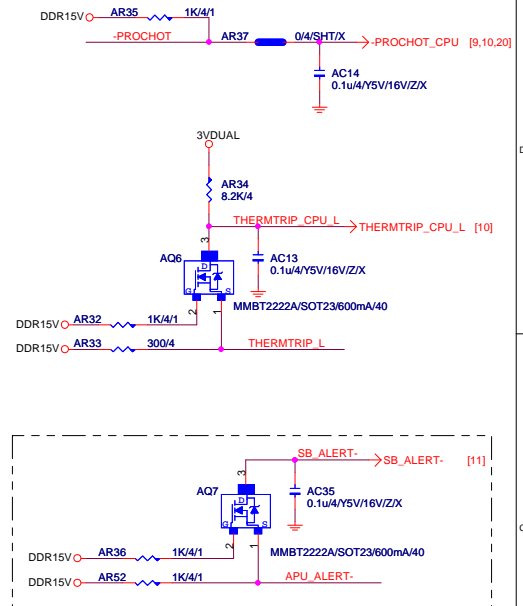
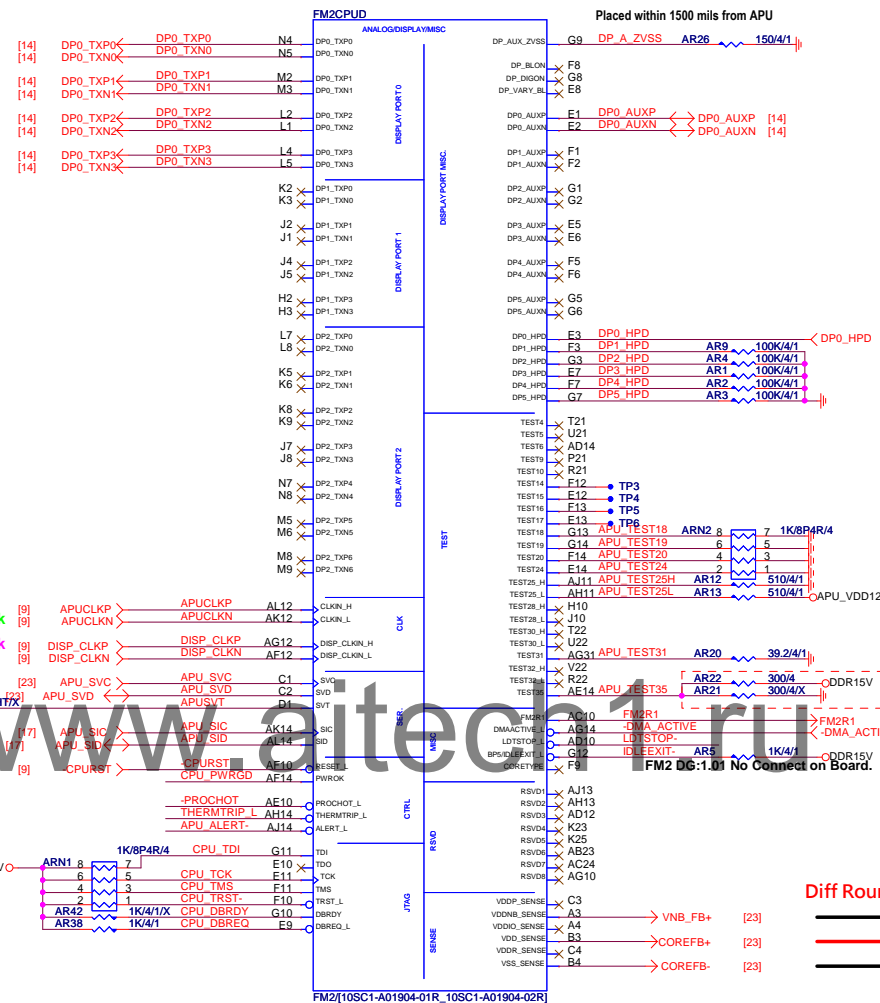
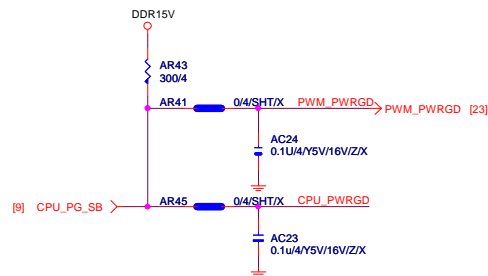
[illegible]

Circuit or PCB layout change for next version

[illegible]





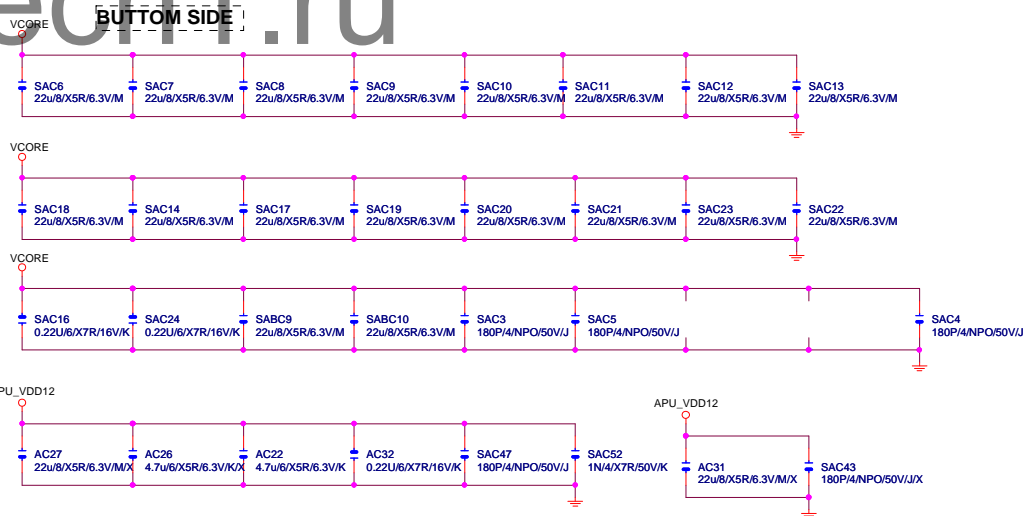
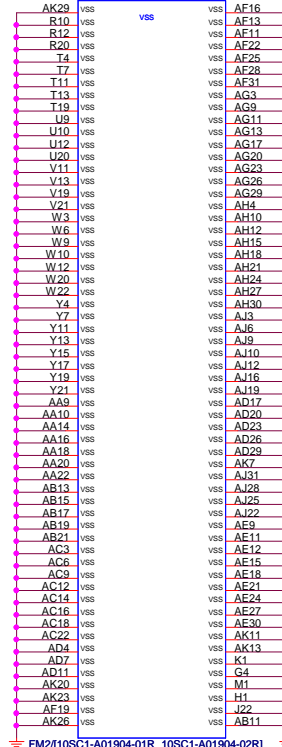


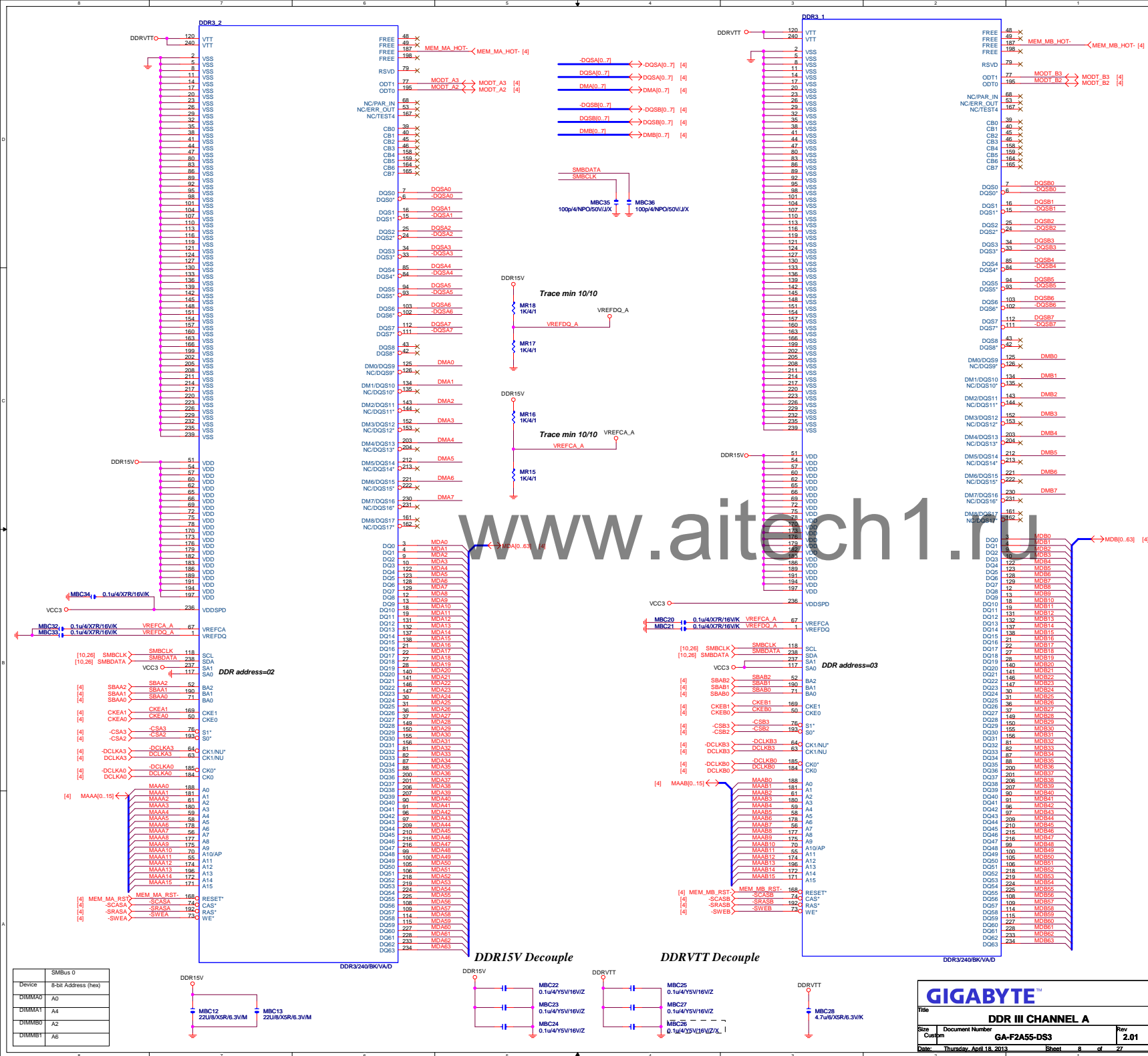
Diff Rount APU to PWM

_____ VNB_FB+
 _____ COREFB-
 _____ COREFB+

	APU FM2
Group A	VDDA25:1.8~2.7V/0.5A
Group A	DDR15V:0.8~2.3V/30A
Group B	VCORE: 0.8~2.0V/120A
Group B	VCORE_NB:1.2V/50A
Group B	VDDP:1.2V/5A
Group B	VDDR:1.2V/5A

Group A must early than Group B

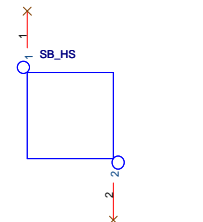






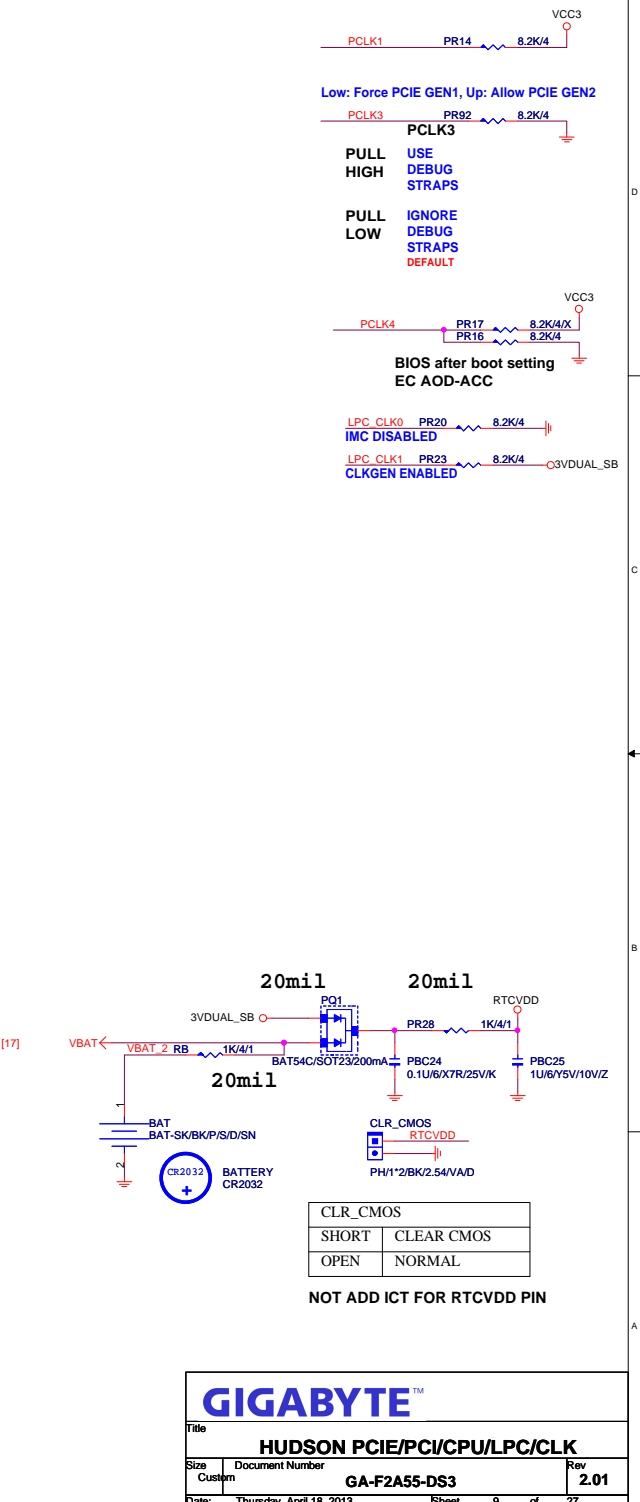
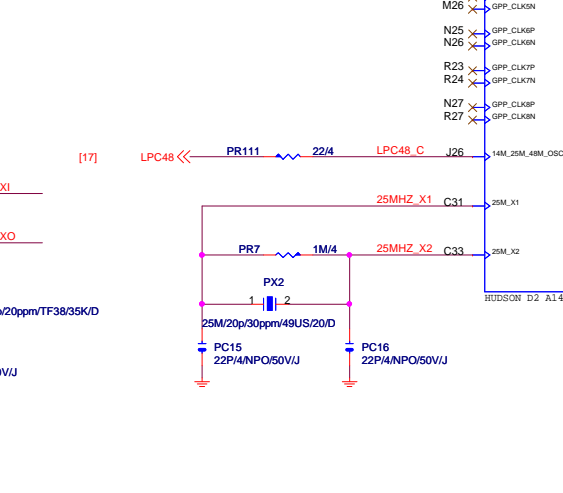
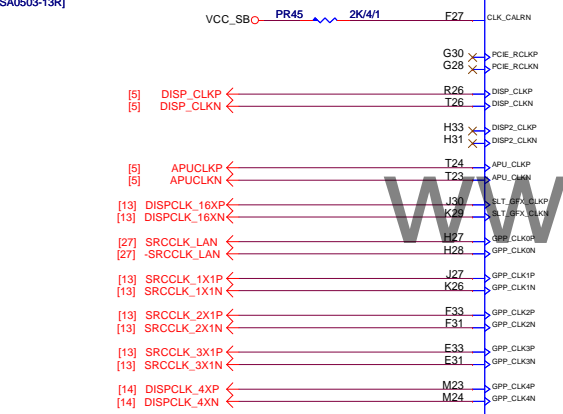
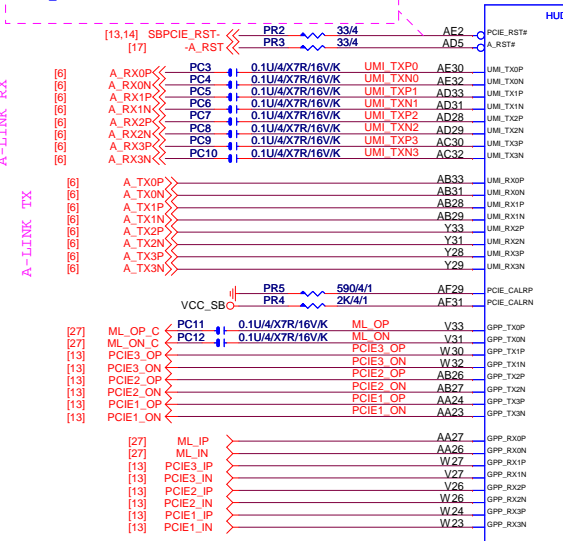
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK



SB_HS 12SP2-SA0503-11R by ECN A11
SB_HS/12SP2-SA0503-11R_12SP2-SA0503-12R_12SP2-SA0503-13R

PCIE_RST# connect to APU PCIe Devices/Slots

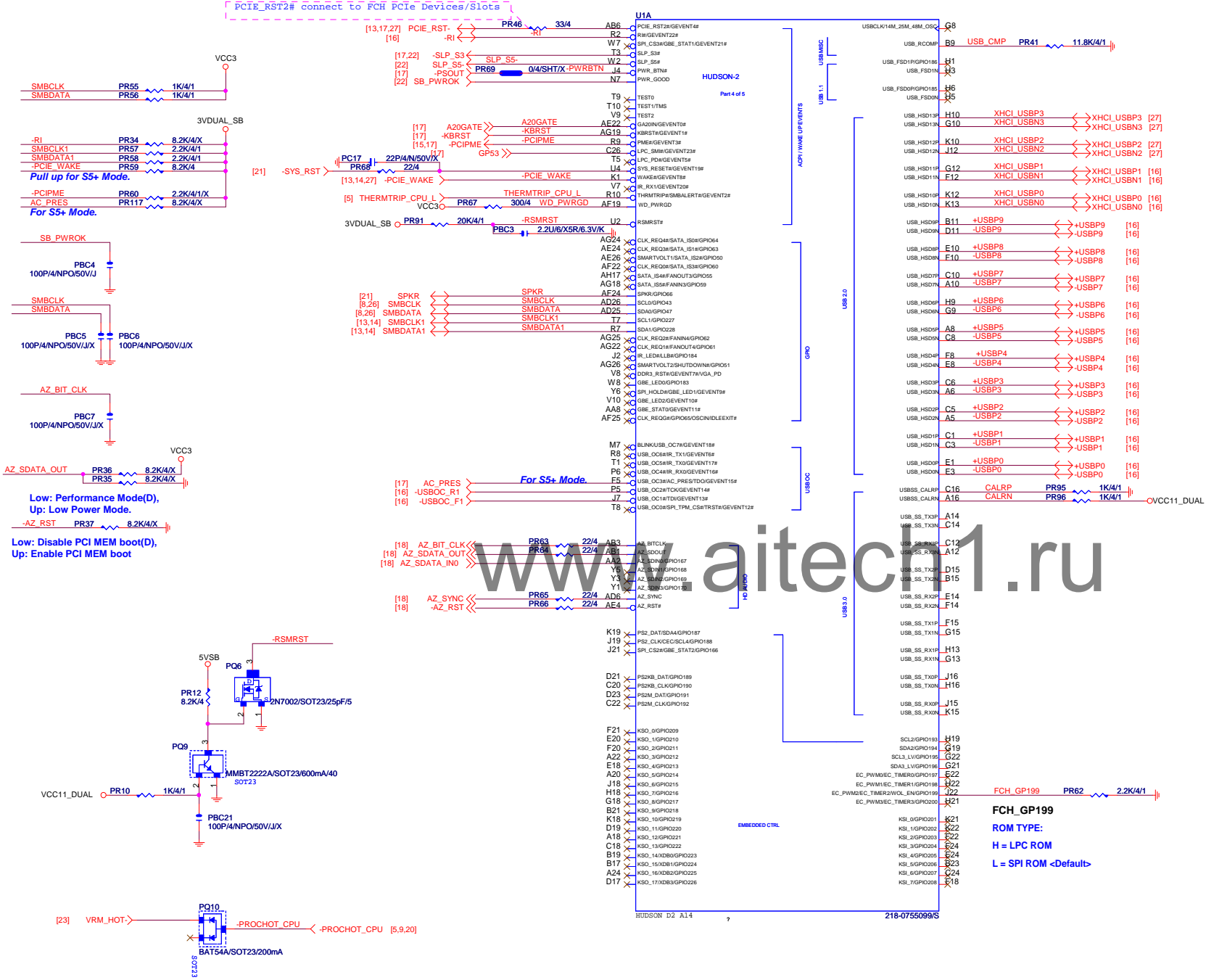


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Title: **HUDSON PCIE/PCI/CPU/LPC/CLK**

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USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	FRONT PANEL
USB2	FRONT PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

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FCH_GP199 PR62 2.2K/4/1

FCH_GP199

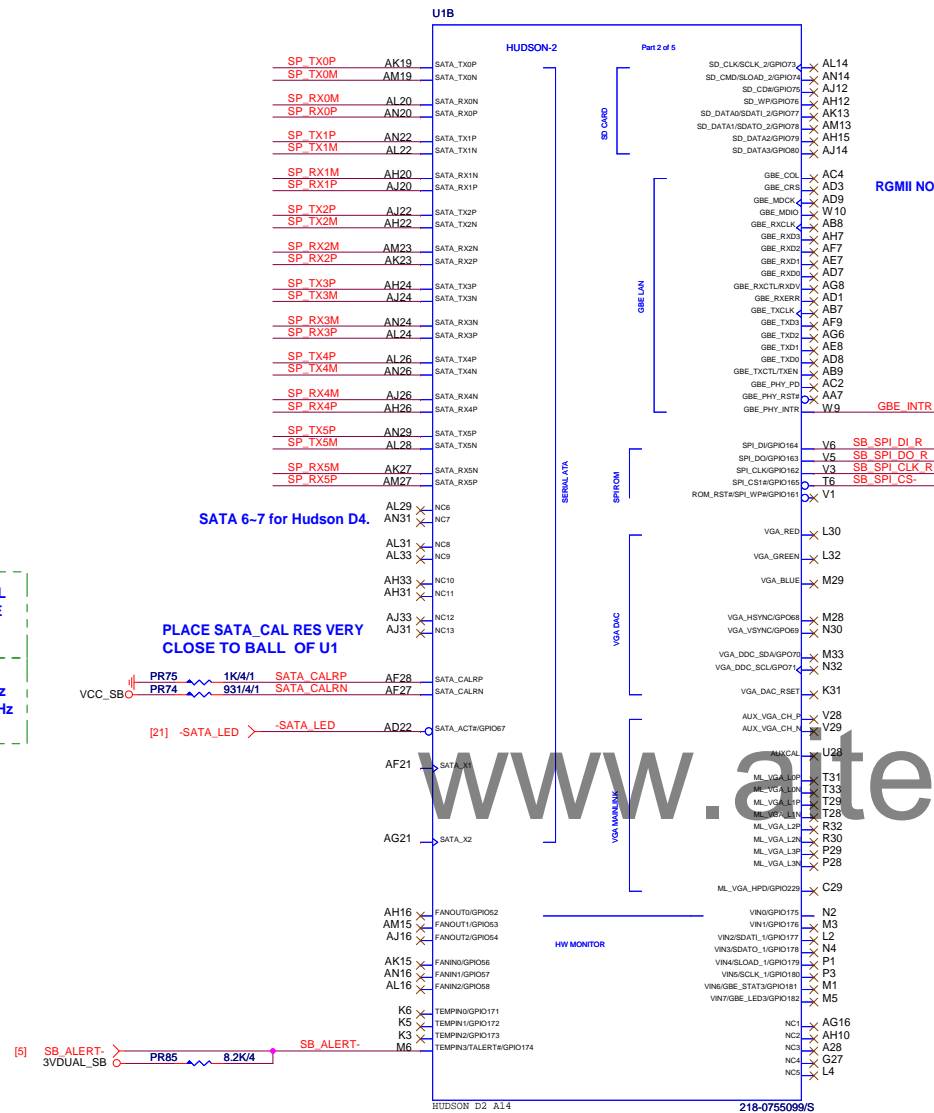
ROM TYPE:

H = LPC ROM

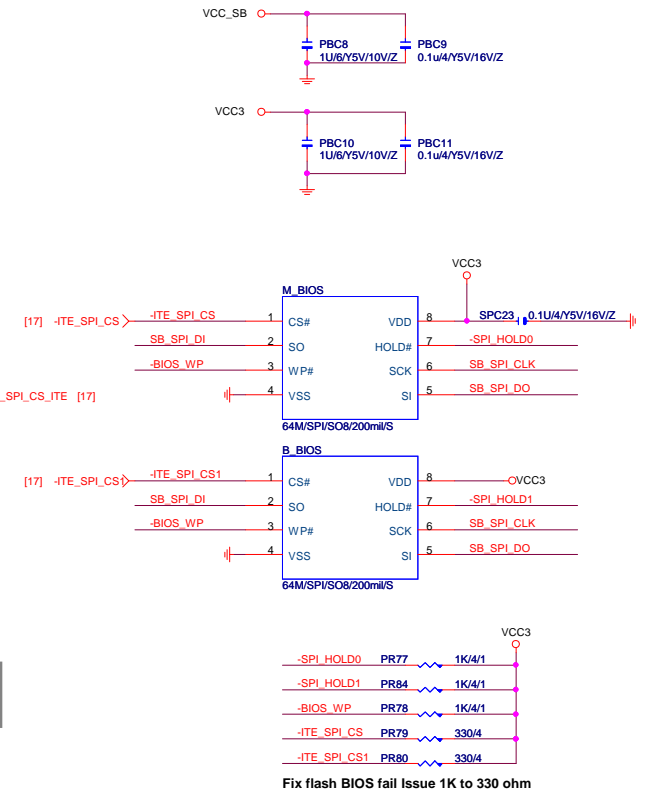
L = SPI ROM <Default>

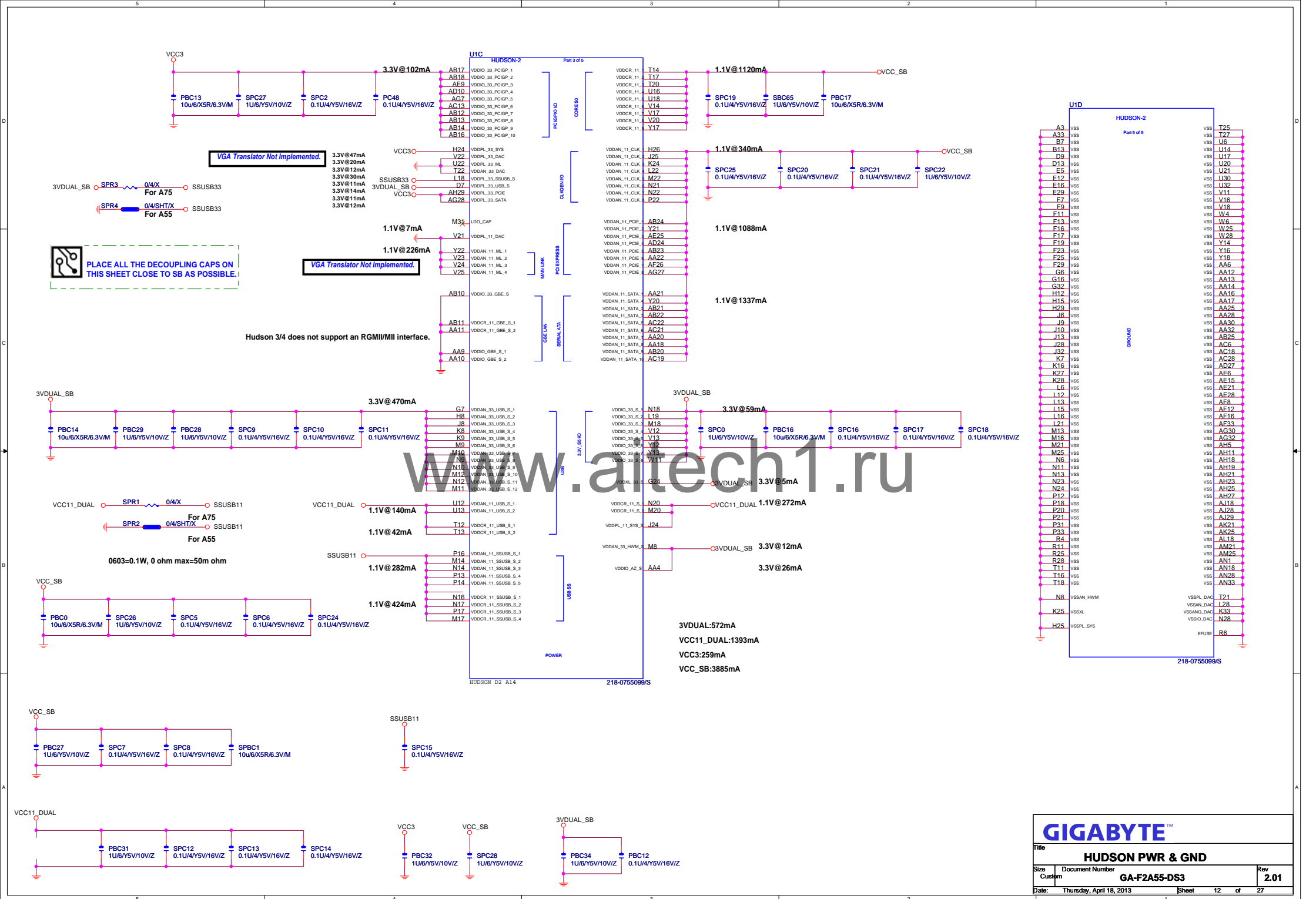
 **PLACE SATA_CAL RES VERY CLOSE TO BALL OF U1**

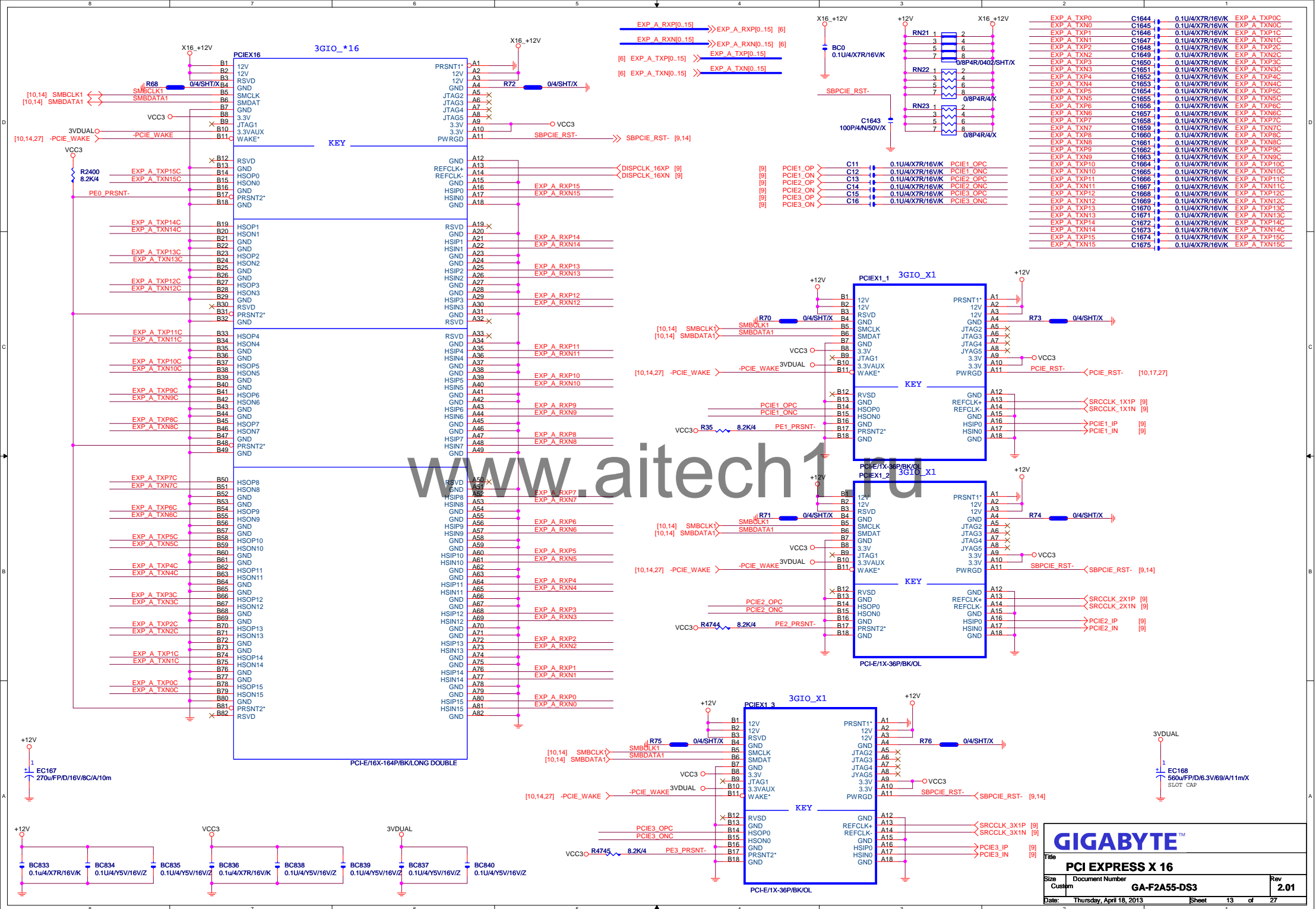
NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK



RGMMI NOT SUPPORT. DG:1.20

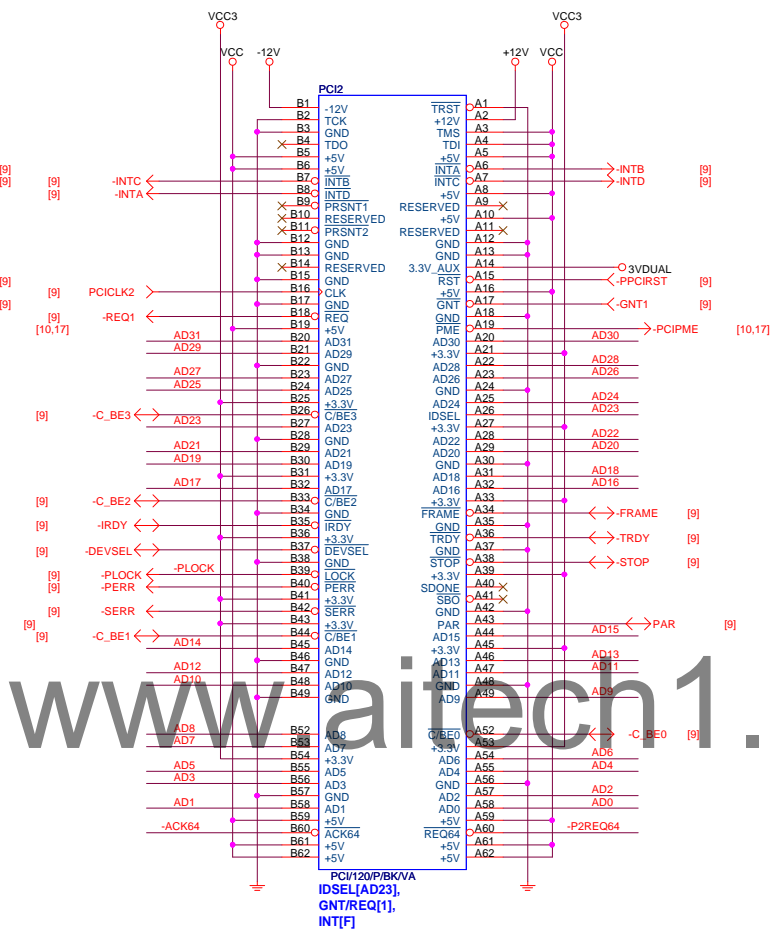
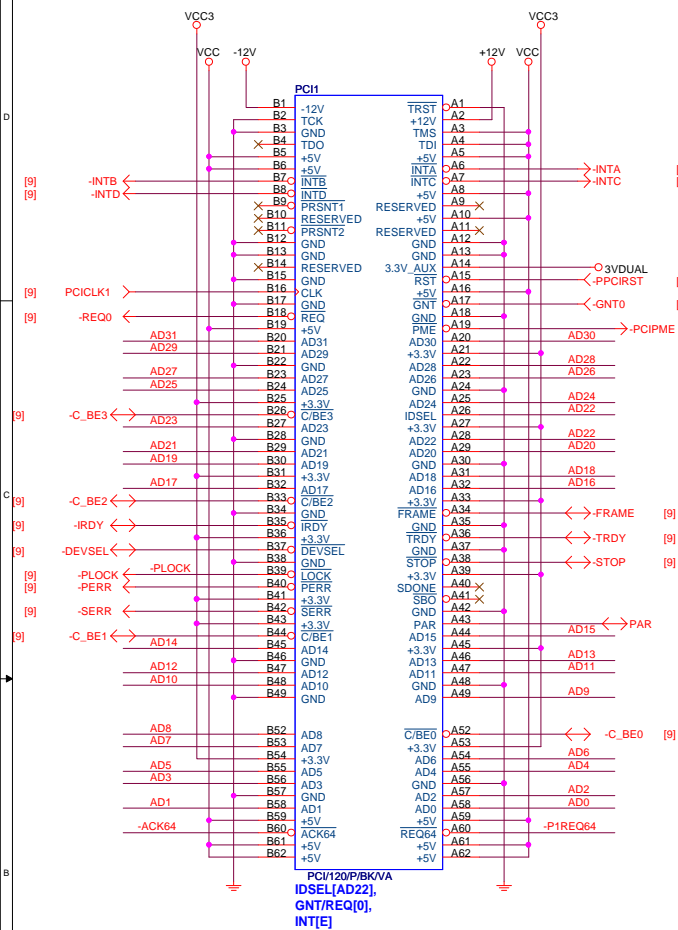




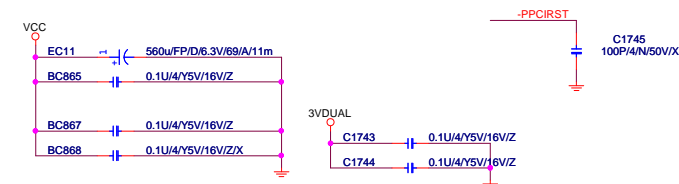
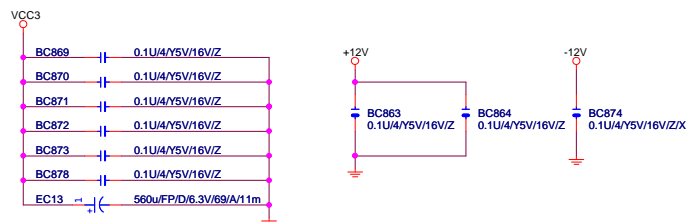


PCI SLOT

[9] AD[0..31] <--> AD[0..31]



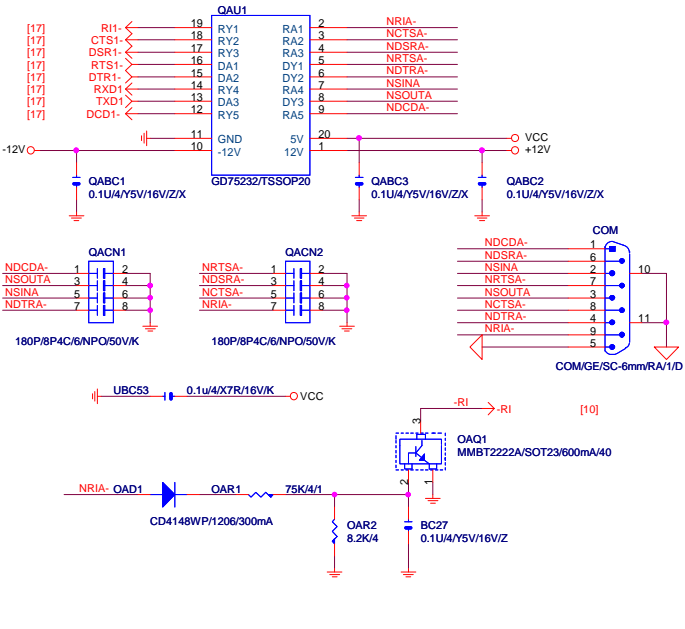
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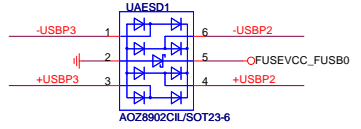
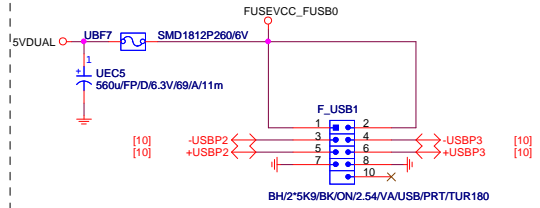
GIGABYTE

Title			PCI SLOT 1,2
Size	Document Number	Rev	
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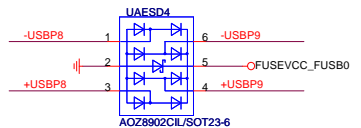
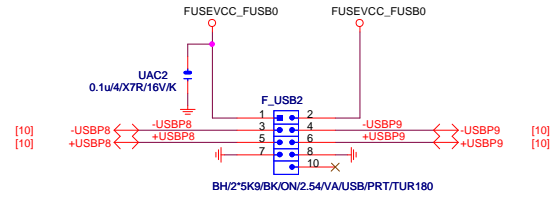
COM PORT



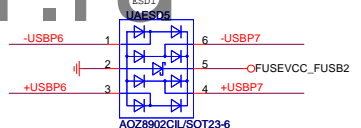
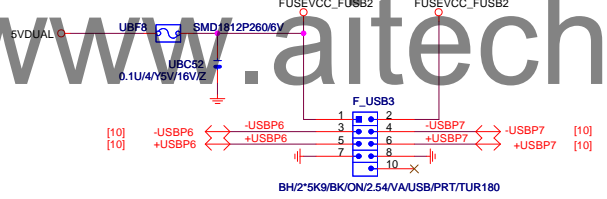
FRONT SIDE USB1



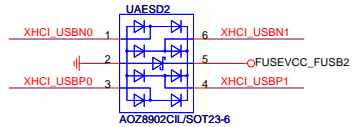
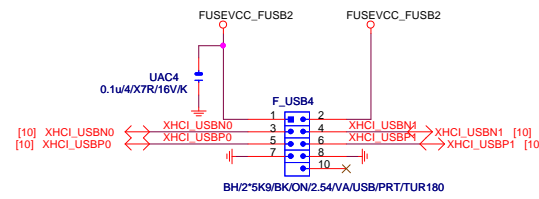
FRONT SIDE USB2



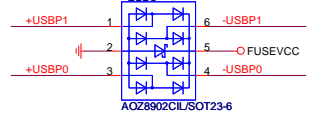
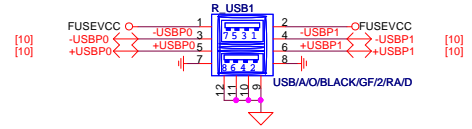
FRONT SIDE USB3



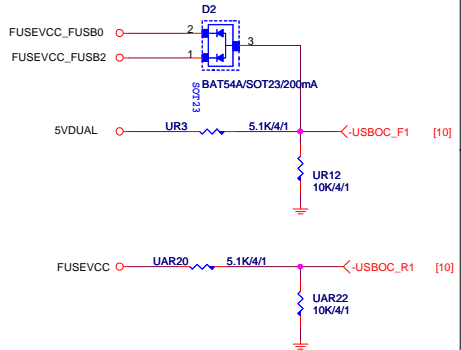
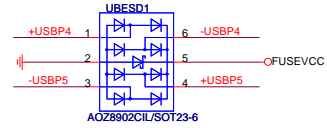
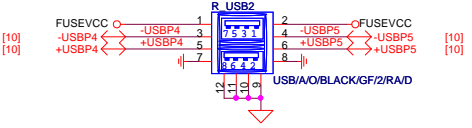
FRONT SIDE USB4

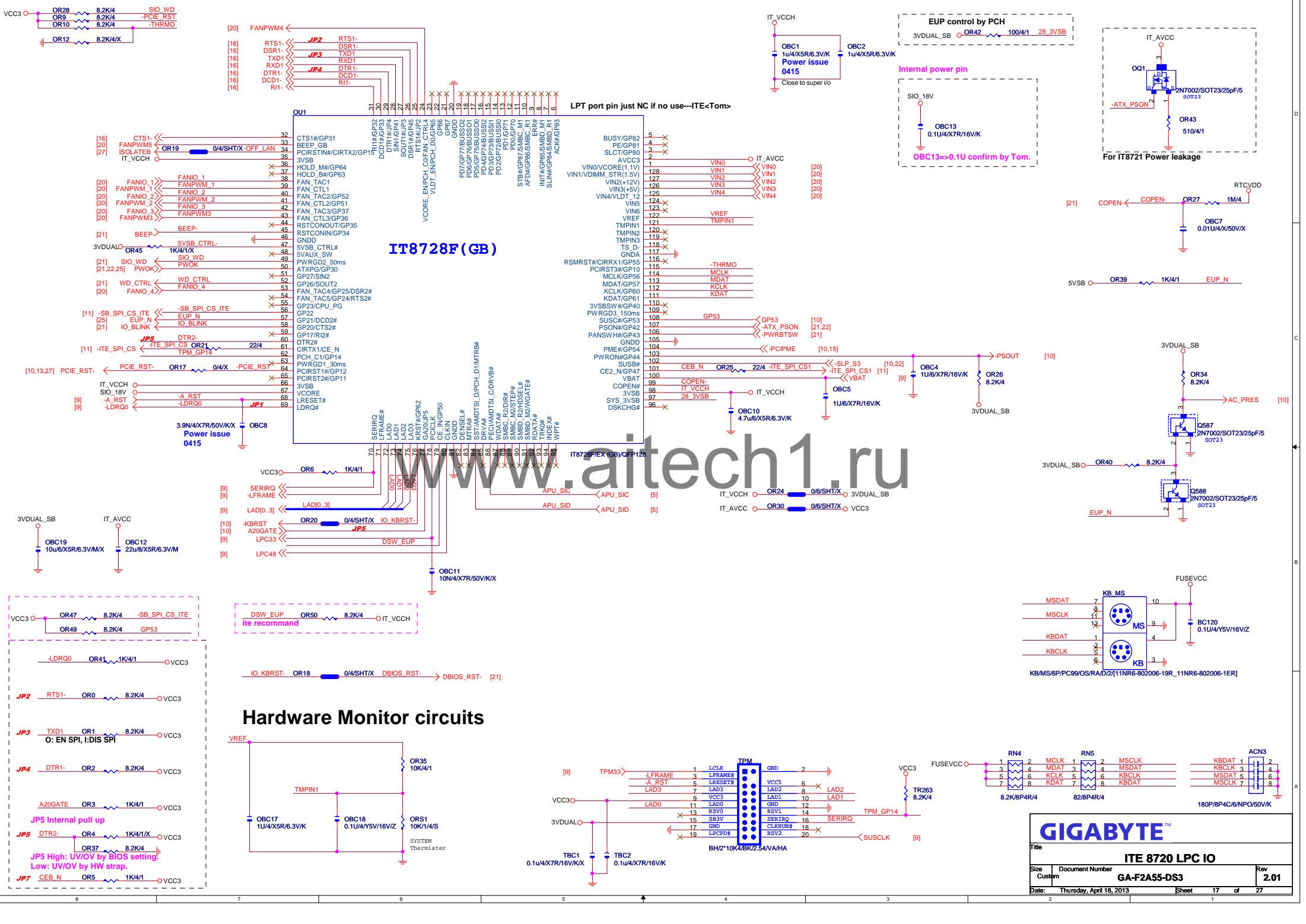


REAR SIDE R_USB1

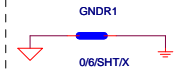


REAR SIDE R_USB2

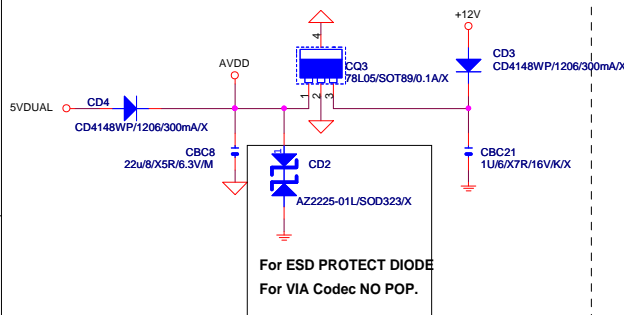
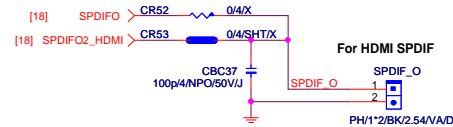




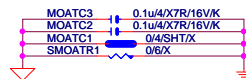
Between Audio to USB_LAN



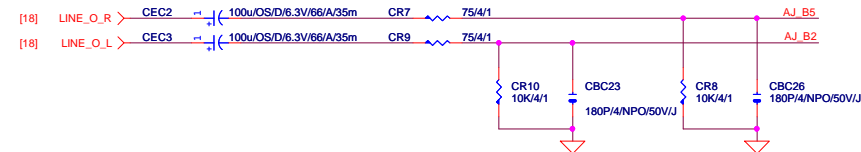
SPDIF



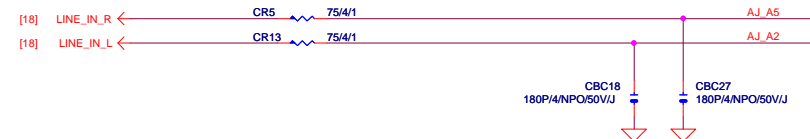
For ESD PROTECT DIODE
For VIA Codec NO POP.



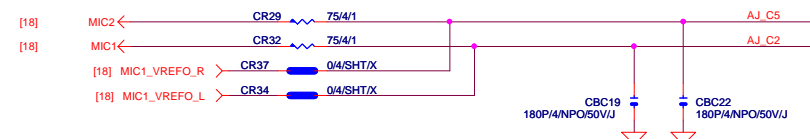
LINE OUT
FRONT OUT



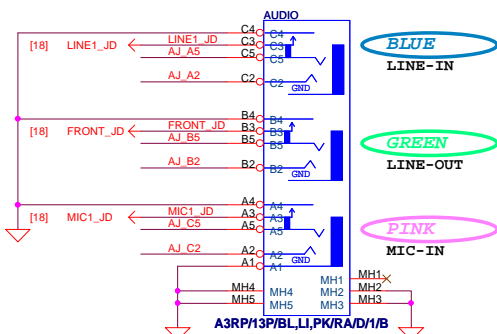
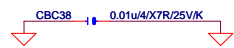
LINE-IN



MIC



For Audio precision test



BLUE
LINE-IN

GREEN
LINE-OUT

PINK
MIC-IN

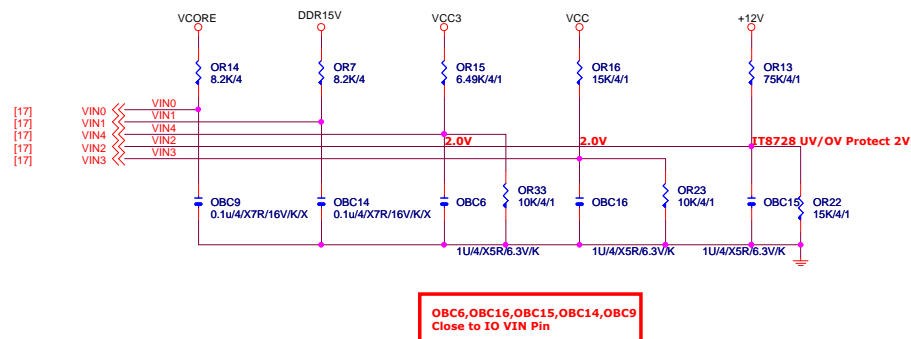
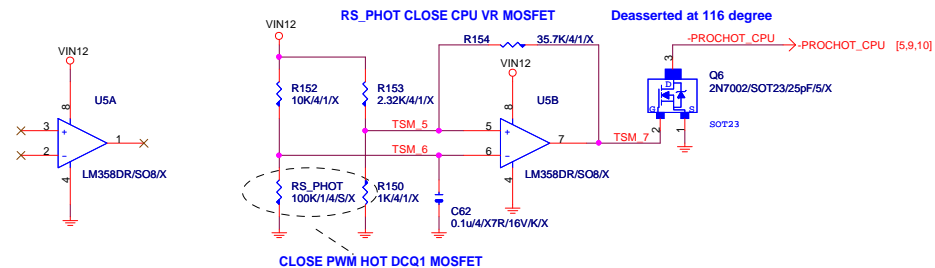
A3RP/13P/BL/LI,PK/RA/D/H/B
A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15P/[11NR6-403004-11]

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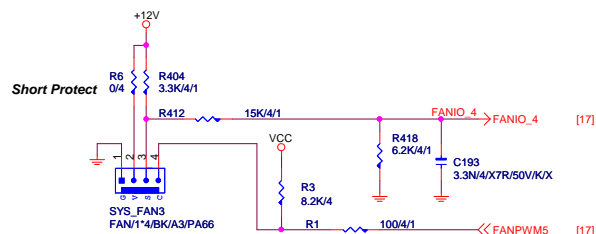
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Title				
AUDIO JACK				
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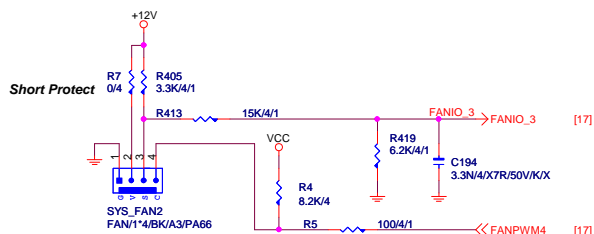
MOSFET HOT



SYSTEM FAN3 PWM MODE

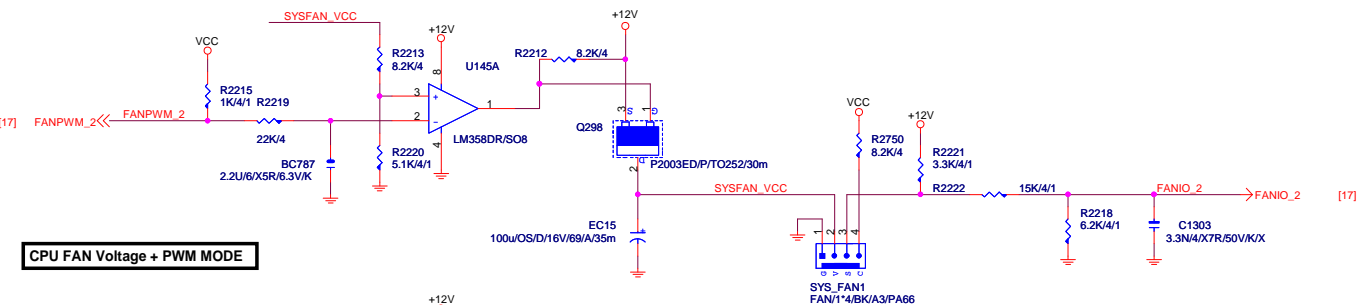


SYSTEM FAN3 PWM MODE

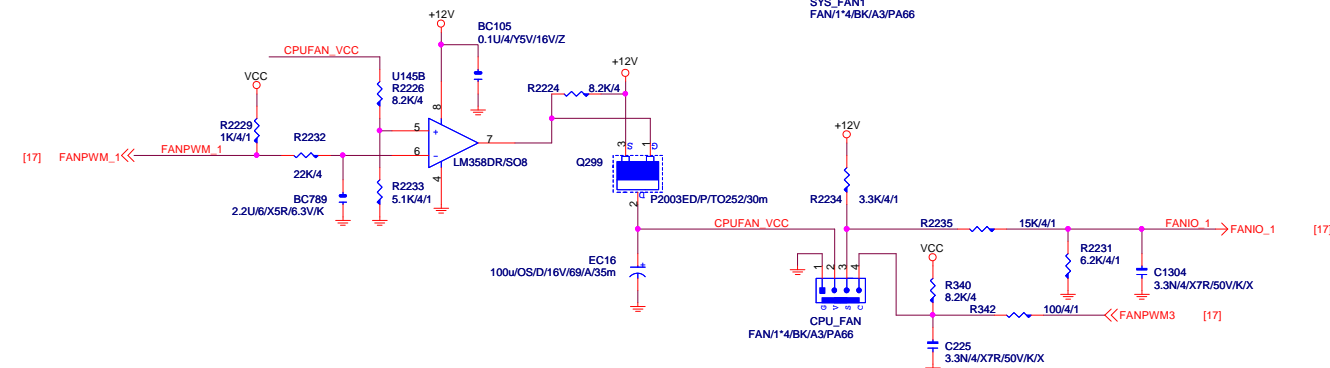


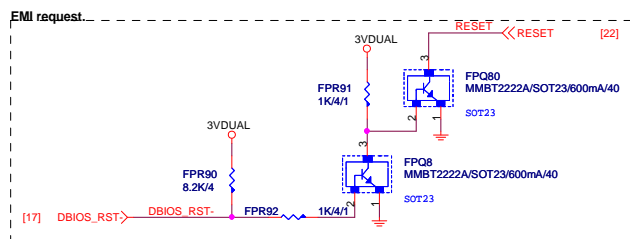
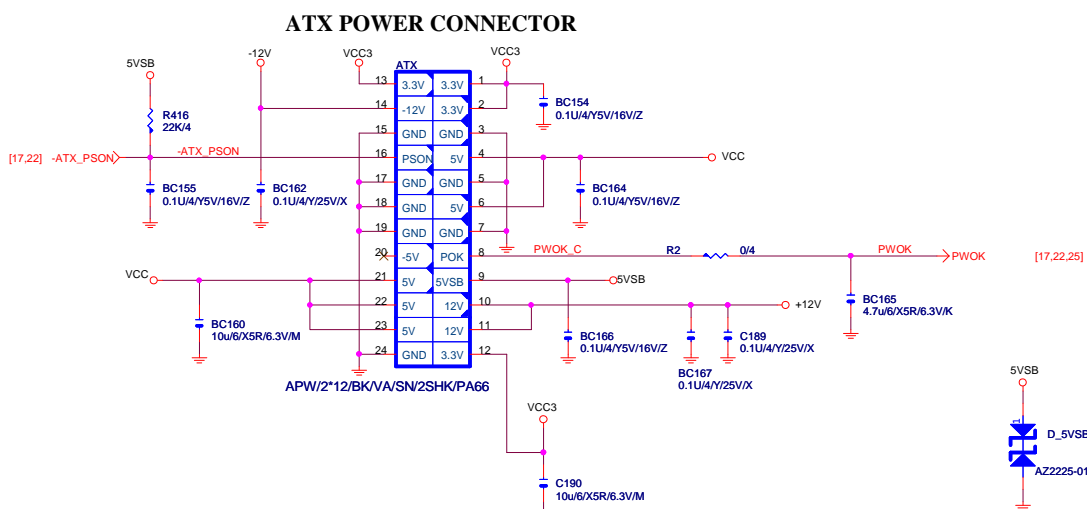
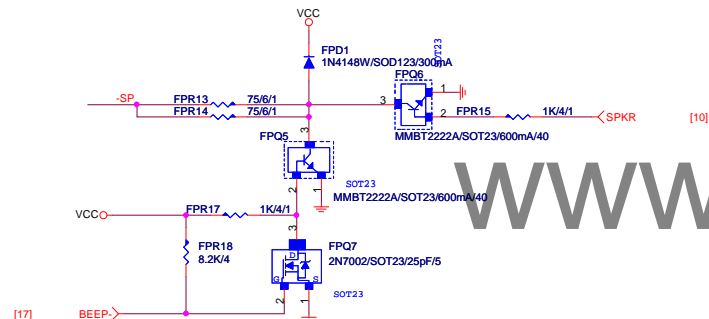
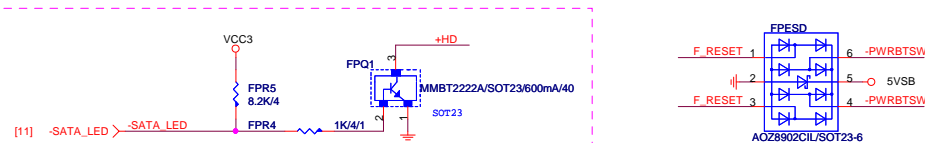
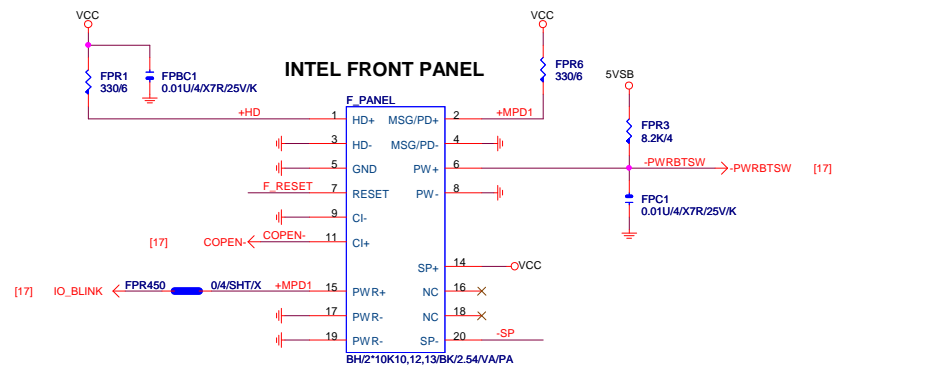
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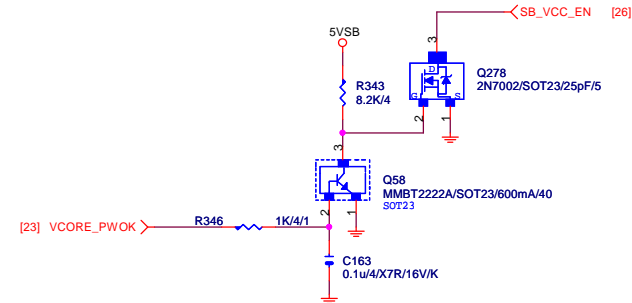
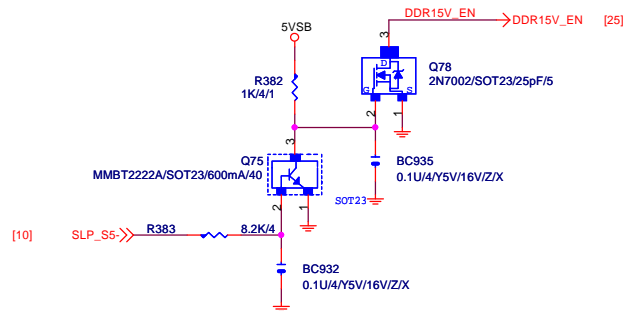
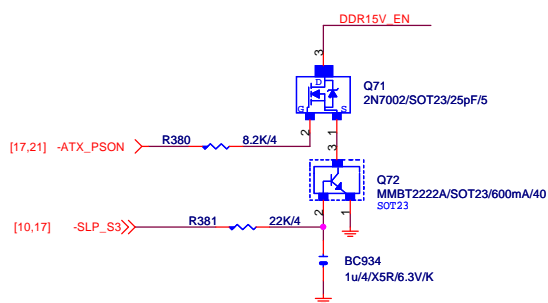
SYSTEM FAN1 Voltage MODE



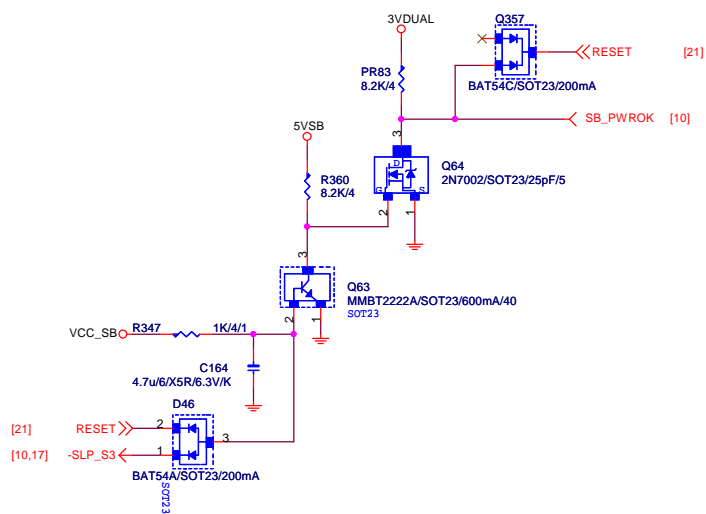
CPU FAN Voltage + PWM MODE



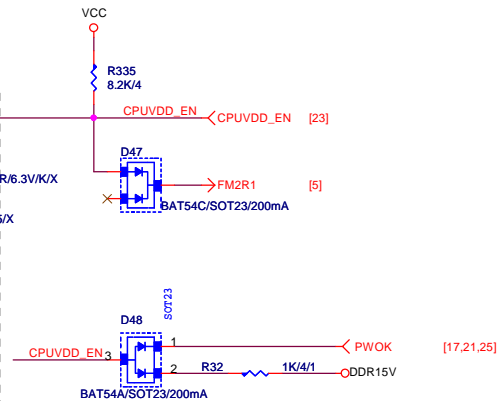
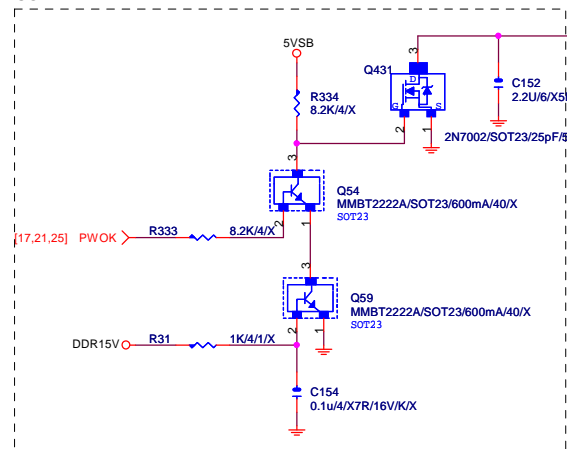




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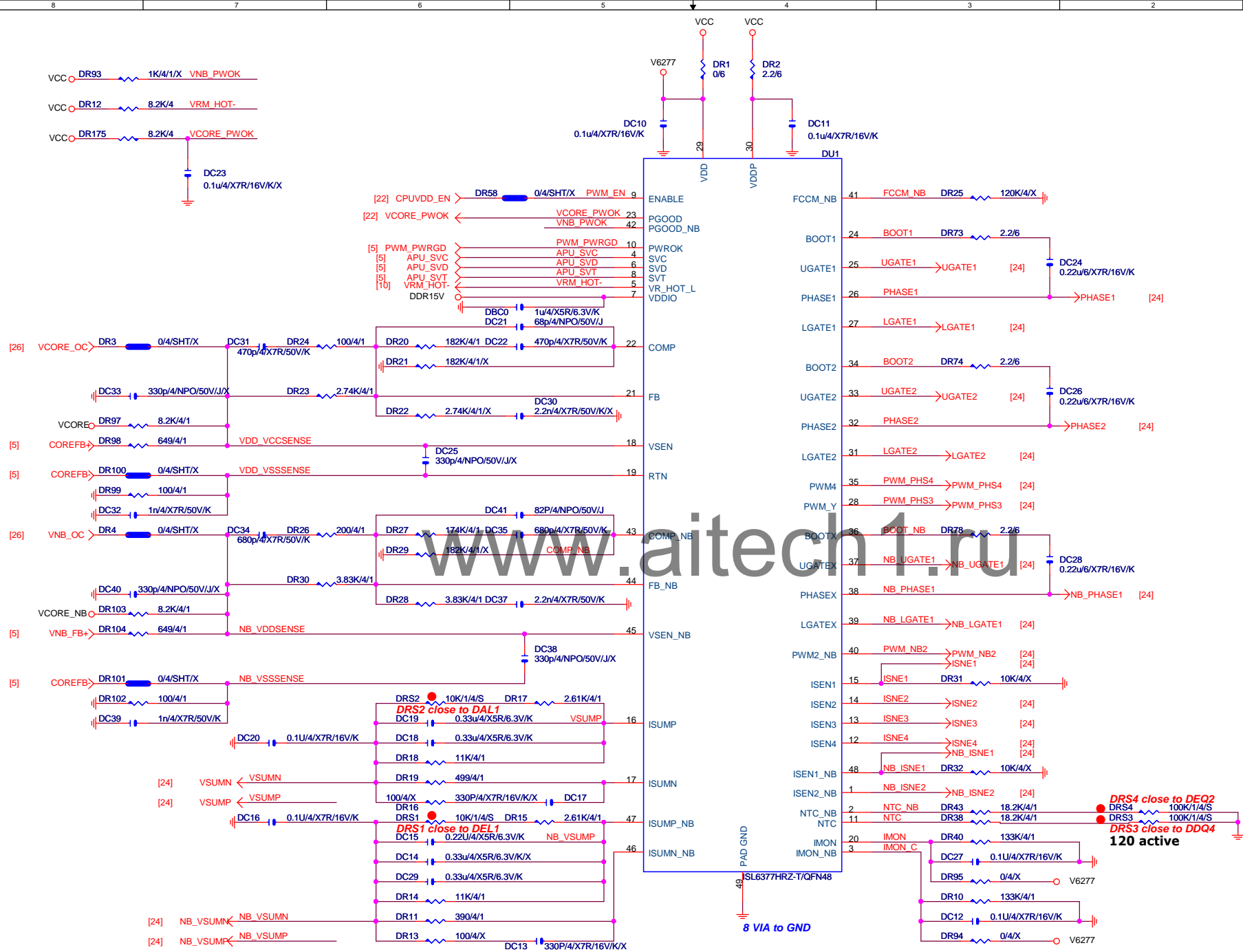


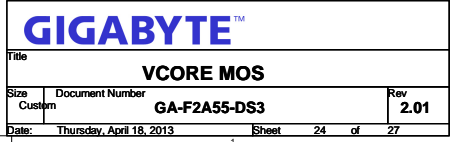
CO-LAY



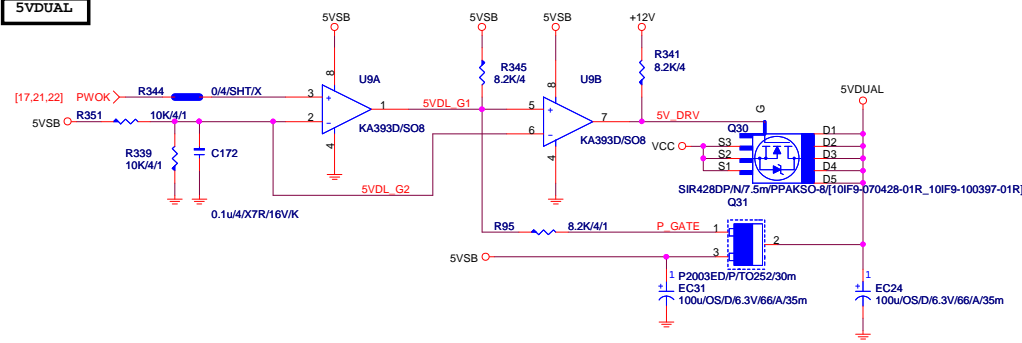
GIGABYTE™

POWER SEQUENCE			
Title	POWER SEQUENCE		
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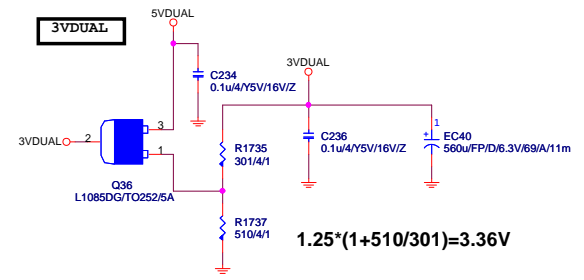




5VDUAL

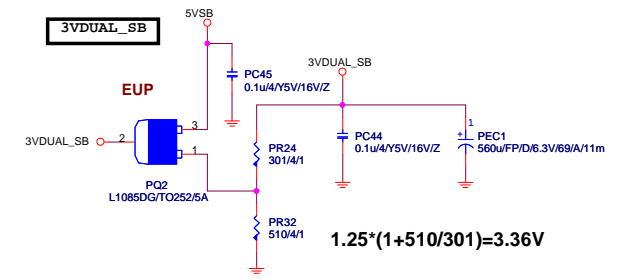


3VDUAL



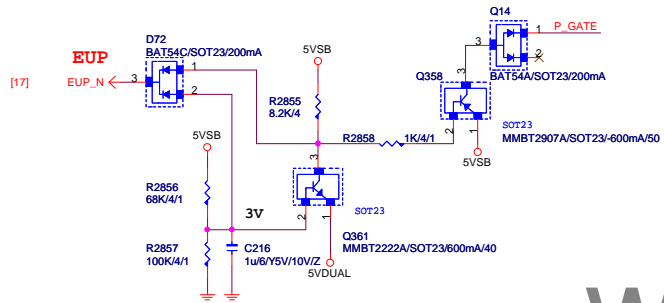
$$1.25 \cdot (1 + 510/301) = 3.36V$$

3VDUAL_SB



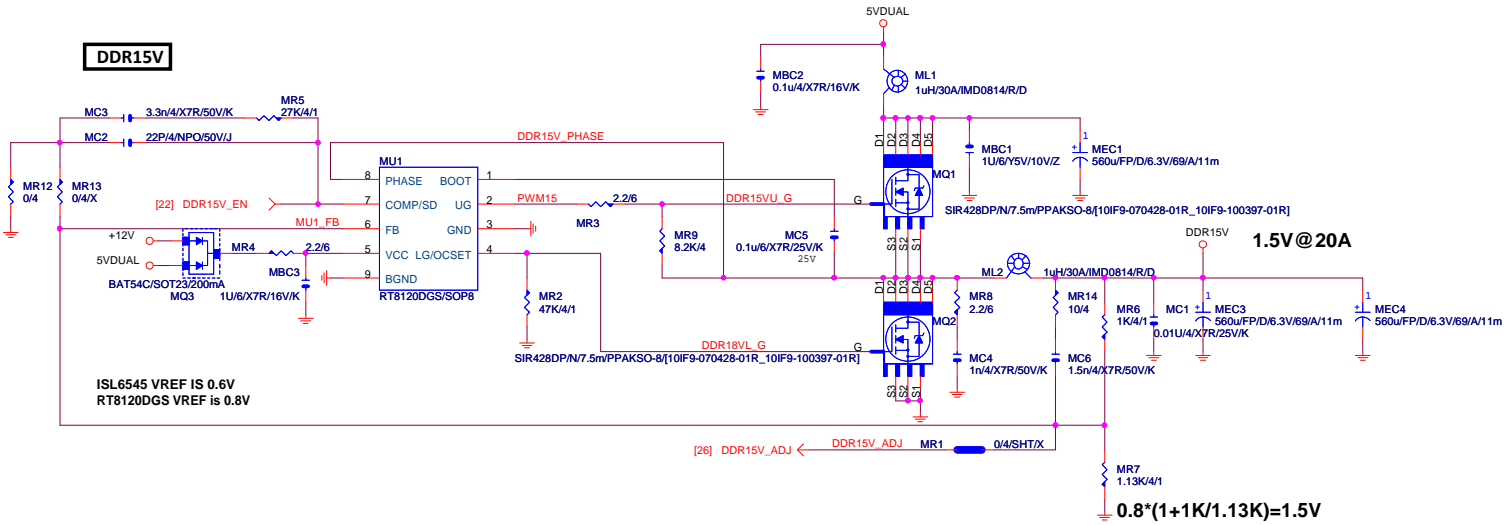
$$1.25 \cdot (1 + 510/301) = 3.36V$$

EUP



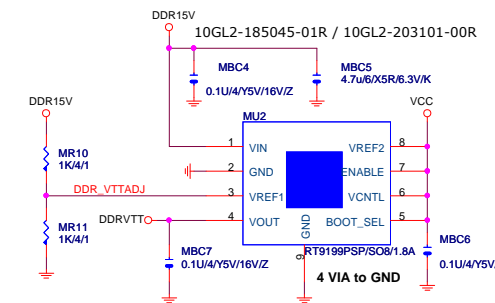
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DDR15V

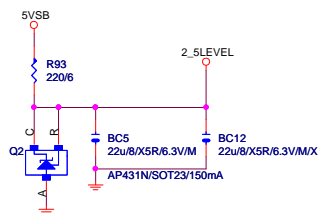
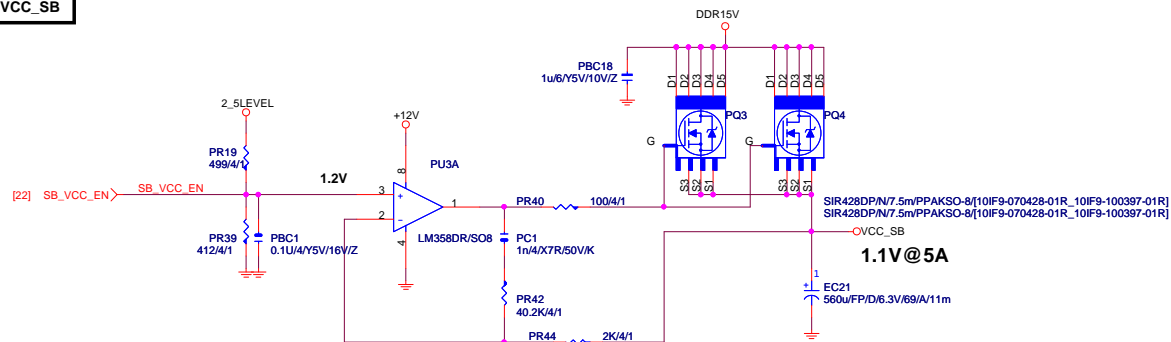


$$1.5V @ 20A$$

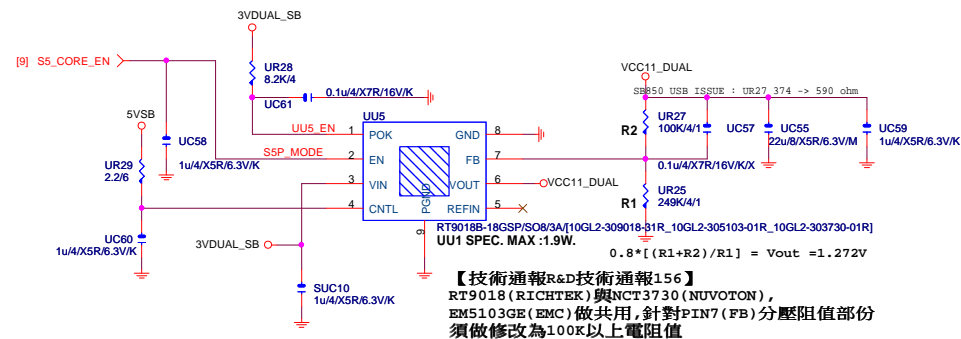
$$0.8 \cdot (1 + 1K/1.13K) = 1.5V$$



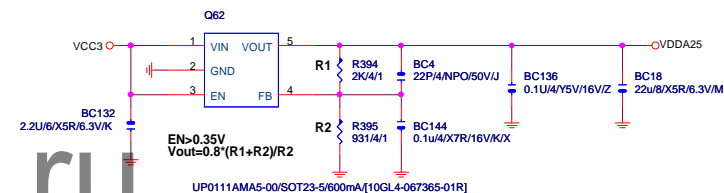
VCC_SB



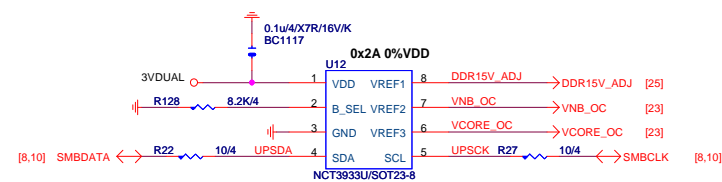
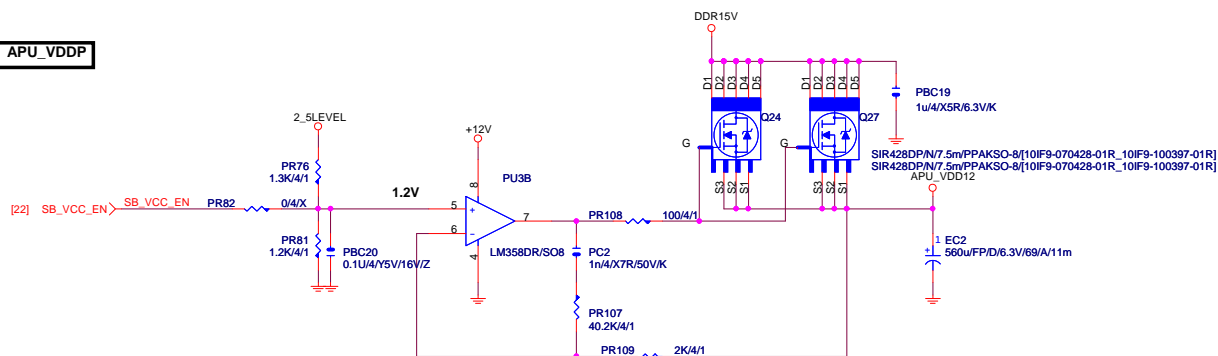
VCC11_DUAL



VDDA25



APU_VDDP



GIGABYTE

Title		SB POWER, APU_VDDP, VDDA25, VCC12Dual	
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